REMARKS

In view of the comments which follow, and pursuant to 37 C.F.R. § 1.111, reconsideration of the Official Action of February 9, 2005 is respectfully requested by Applicants.

Summary

Claims 1- 10 stand rejected, and are pending following entry of the present remarks.

Rejection under 35 U.S.C. § 102 (e)

Claim 1 was rejected under 35 U.S.C. § 102 (e) as being anticipated by Belser et al. (US Patent 5,737,344). Applicants respectfully traverse these rejections.

Claim 1 is directed to a disk device, which comprises a disk drive, and a host computer.

Claim 1 recites that the processing circuit of the disk drive includes a low-level error-correction code unit for performing error correction of the data written to a physical address corresponding to a single sector of the disk, and the host computer includes a high level error correction code unit for performing error correction of the read data supplied through the interface and read from more than one sector of the disk. Thus, as claimed, a low-level error correction is performed by the processing circuit of the disk drive, and a high-level error correction is performed by the host computer.

The Examiner states that Belser discloses error correction for a data read from a disk drive by using parity sectors whenever a sector-level ECC process is unsuccessful (column 6, lines 61 -67). However, Belser fails to teach or suggest whether the ECC process is performed at the disk drive level and whether the parity sector correction is performed at the host computer level.

The Examiner further states that Belser' s ECC unit (214) is a low level error correction unit, and that Belser' s high level error correction processing can be performed by the host computer. Applicants respectfully disagree. Belser discloses in regard to the tasks (600) that the generating and storing of parity sectors may also be performed by a host computer (column 5, lines 63 – 66). However, Belser does not

disclose that a low-level error correction is performed by a processing circuit of a disk drive, and a high-level error correction is performed by the host computer.

In regard to Belser' s disclosure that the parity block may include two or more parity computations, Applicants submit that Belser fails to teach or suggest that these multi-parity computations are performed at a specific location, such as the host computer.

Accordingly, for at least the above discussed reasons, Claim 1 is not anticipated by Belser. Independent Claims 4 and 10 are also allowable over Belser for reciting the same distinguishable feature of Claim 1. Claims 3 – 9, which are dependent on Claim 4, either directly or indirectly, are also allowable for at least the same reasons.

Rejection under 35 U.S.C. § 103(a)

Claims 1 and 4 – 10 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Belser (US 6,021,463, "Belser '463") in view of Belser et al. (US Patent 5,737,344; "Belser '344"). Applicants respectfully traverse these 103(a) rejections.

Claim 1 recites that the processing circuit of the disk drive includes a low-level error-correction code unit for performing error correction of the data written to a physical address corresponding to a single sector of the disk, and the host computer includes a high level error correction code unit for performing error correction of the read data supplied through the interface and read from more than one sector of the disk.

Applicants submit that both references fail to teach or disclose the Claim 1 arrangement that low-level error correction is performed by a processing circuit of a disk drive, and a high-level error correction is performed by the host computer.

As discussed above in regard to the 102(e) rejection, the arrangement of Claim 1 is distinguished from Belser '344.

In this 103(a) rejection, the Examiner states that Belser '463 discloses a high level correction performed by a disk drive processor (9) to correct data of multiple sector-level-ECC-uncorrectable sectors. The Examiner concludes that the ECC

system of Belser '463 can be modified by placing the second (high) level ECC processing in the host computer instead of the disk drive processor. Thus, the Examiner acknowledges that Belser '463 does not teach or suggest the claimed arrangement of Claim 1.

Accordingly, both of Belser references may not properly be combined to reject Claim 1.

Similar discussions can show that independent Claims 4 and 10 may not be rejected by a combination of the '344 and '463 Belser' s references. Dependent Claims 5 – 9 are also allowable for at least the same reasons.

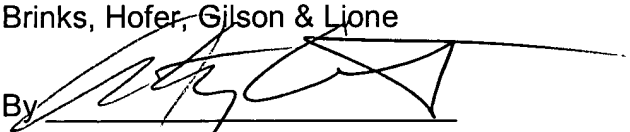
Accordingly, Applicants respectfully request that the claim rejections under 35 USC 103(a) be withdrawn.

Conclusion

Applicants respectfully submit that claims 1 – 10 are in condition for allowance, and such action is earnestly submitted. Applicants believe that a two-month extension is due, and a corresponding check is enclosed. If, there are additional fees due, Applicants request that this paper constitutes any necessary petition and authorizes the Commissioner to charge any underpayment, or credit any overpayment, to Deposit Account No. 23-1925.

If any issues remain, Applicants request that the Examiner call the undersigned to expedite the prosecution of the application.

Respectfully submitted,
Brinks, Hofer, Gilson & Lione

By 

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